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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,162	07/28/2003	Sander L. Gierkink	S. GIERKINK 2-2	4343

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EXAMINER	
HANNON, CHRISTIAN A	

ART UNIT	PAPER NUMBER
2618	

NOTIFICATION DATE	DELIVERY MODE
04/10/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docket@hittgaines.com

Office Action Summary	Application No.	Applicant(s)	
	10/628,162	GIERKINK ET AL.	
	Examiner	Art Unit	
	CHRISTIAN A. HANNON	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-11,13-18 and 20-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-11,13-18 and 20-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is response to applicant's response filed on 1/4/2008. Claims -4, 6-11, 13-18 and 20-23 are now pending in the present application. **This action is made final.**

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 & 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al (US 7,079,860), hereinafter Yamamoto, in view of Pugel et al (US 6,553,216), hereinafter Pugel.

Regarding claims 1 & 8, Yamamoto teaches a phase-error suppressor for use with a plurality of transistors having a common source coupled to a current generator and configured to receive signals at a frequency (Figure 12, Items 201, 202, 115; Yamamoto) comprising, an inductor, coupled between said common source, of which has an inherent associated capacitance, and said current generator, (Figure 12, Item 221; Yamamoto) and a capacitor coupled to said inductor and coupled in parallel to said current generator, said capacitor being configured to shunt said inductor to ground at a selected radio frequency (Figure 12, Item 211; Yamamoto) (Column 13, Lines 60-64; Column 14, Lines 13-19, Lines 37-43; Yamamoto). However Yamamoto fails to explicitly teach that the inductor is configured to resonate proportionally to said

frequency with a first capacitance associated with said plurality of transistors. Pugel teaches that a value of an inductor may be selected so as to cause a resonance between an associated FET's capacitance and the inductor (Column 10, Lines 31-51; Pugel). Therefore it would have been obvious in light of Yamamoto's teaching of selection of an inductor's value to include the teaching of Pugel in order to tune out the parasitic capacitance at the drain of the FET, to thereby decrease the loading effect due to the parasitic capacitance. Furthermore since claim 8 is merely a method recitation of claim 1, claim 8 is rejected on the same grounds.

3. Claims 2-4, 6, 7, 9-11 & 13-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto in view of Pugel and further in view of Sano et al (US 5,884,154), hereinafter Sano.

Regarding claims 2 & 9, Yamamoto & Pugel teach the device and method of claims 1 & 8, however Yamamoto & Pugel fail to teach wherein said plurality of transistors and said current generator form a portion of a system selected from a group consisting of a quadrature oscillator buffer, a quadrature oscillator and a quadrature mixer. Sano teaches a plurality of transistors and said current generator form a portion of a system selected from a group consisting of a quadrature oscillator buffer (Figure 1, items 51, 53, VDD, Q14, 41,43,45,47,15,19 & 25; Sano), a quadrature oscillator (Column 3, Lines 35-39; Sano) and a quadrature mixer (Column 3, Lines 25-27; Sano). Therefore it would have been obvious to combine a RF communication system out of Yamamoto & Pugel's amplifier/mixers and Sano's mixer in order to create a low noise

high linearity system as Sano suggests (Column 2, Lines 35-38; Sano). Furthermore since claim 9 is merely a method recitation of claim 2, claim 9 is rejected on the same grounds.

With regards to claims 3 & 10, Yamamoto & Pugel teach the phase-error suppressor of claims 1 & 8, however Yamamoto & Pugel fail to teach wherein said inductor and said first capacitance resonate at twice said frequency. Sano teaches wherein said inductor and said first capacitance resonate at twice said frequency (Column 4, Lines 3-5, 10-12 and 23-44; Sano). Therefore it would have been obvious to combine a RF communication system out of Yamamoto & Pugel's amplifier and Sano's mixer in order to create a low noise high linearity system as Sano suggests (Column 2, Lines 35-38; Sano). Furthermore since claim 10 is merely a method recitation of claim 3, it is rejected on the same grounds.

Regarding claims 4 & 11, Yamamoto & Pugel teach the phase error suppressor of claims 1 & 8, however Yamamoto & Pugel fails to teach wherein said first capacitance is dominated by a base-to-emitter capacitance of at least one of said plurality of transistors. Sano teaches wherein said first capacitance is dominated by a base-to-emitter capacitance of at least one of said plurality of transistors (Column 3, Lines 39-45; Sano). Therefore it would have been obvious to combine a RF communication system out of Yamamoto & Pugel's amplifier and Sano's mixer in order to create a low noise high linearity system as Sano suggests (Column 2, Lines 35-38; Sano). Furthermore since claim 11 is merely a method recitation of claim 4, it is rejected on the same grounds.

In regards to claims 6 & 13, Yamamoto & Pugel teach the phase error suppressor of claims 1& 8, however Yamamoto & Pugel fail to teach wherein said frequency is at least three GHz. Sano teaches wherein said frequency is at least three GHz (Column 5, Lines 43-46; Sano). While Sano mentions in particular an example of an operating frequency of 880MHZ in one example (Column 5, Lines 9-19), he does not limit the operating frequency to this particular specific frequency and goes on to teach the use of the circuit in a wireless telephone, obvious to one of ordinary skill in the art, which could operate at at least three GHz. Therefore it would have been obvious to combine a RF communication system out of Yamamoto & Pugel's amplifier and Sano's mixer in order to create a low noise high linearity system as Sano suggests (Column 2, Lines 35-38; Sano). Furthermore since claim 13 is merely a method recitation of claim 6, it is rejected on the same grounds.

With regards to claims 7 & 14, Yamamoto & Pugel teach the phase error suppressor of claims 1 & 8, however Yamamoto & Pugel fail to teach where said signals are four periodic local oscillator signals having a 90-degree phase difference. Sano teaches where said signals are four periodic local oscillator signals having a 90 degree phase difference (Column 2, Lines 33-35; Sano). Therefore it would have been obvious to combine a RF communication system out of Yamamoto & Pugel's amplifier and Sano's mixer in order to create a low noise high linearity system as Sano suggests (Column 2, Lines 35-38; Sano). Furthermore since claim 14 is merely a method recitation of claim 7, it is rejected on the same grounds.

Regarding claims 15-21, therein recited are the limitations previously disclosed in apparatus and method claims 1-7 & 8-14, respectively, with the addition that the circuitry details are now made to comprise within an image-rejecting down-converter for use with a RF receiver. Yamamoto & Pugel or Yamamoto in combination with Pugel & Sano teach all the limitations as previously rejected above in addition to the circuit being used within an image-rejecting down-converter for use with an RF receiver (Column 5, Lines 43-46; Sano) obvious to one of ordinary skill in the art Yamamoto would be applied to a receiver structure and therefore one would be motivated to implement the teachings of Sano with Yamamoto to form an image rejected down converter in order to add the benefit of lower noise in the receiver.

4. Claims 22 & 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto in view of Pugel and further in view of Madni et al (US 6,876,843), hereinafter Madni.

Regarding claims 22 & 23, Yamamoto and Pugel teach claim 1, however they both fail to teach where the amount of transistors is greater than two or specifically four. Madni teaches a low noise amplifier with four transistors for use in a differential system (Column 2, Lines 49-56; Madni; Figure 1). Therefore it would have been obvious to combine the teachings of Yamamoto and Pugel with those of Madni in order to implement a LNA in a differential system in order to take advantage of the high Common Mode Rejection Ratio provided by a differential amplifier.

Response to Arguments

5. Applicant's arguments filed 1/4/2008 have been fully considered but they are not persuasive.

Regarding claim 1 the applicant's argument's focus on the incorporation of the Pugel reference into the Yamamoto teachings, asserting that they perform different from the claimed invention. First off the examiner wishes to clarify that the structure and function of the claimed capacitor and those teachings of the prior art of Yamamoto establish the foundation of the current rejection found in this and the preceding office action. Therefore that leaves the only deficiency in the Yamamoto art, that it fails to teach an "inductor configured to resonate proportionally to a frequency with a first capacitance associated with a plurality of transistors." The examiner has relied on the singular teaching of Pugel that an inductor may be used to "tune-out" the parasitic capacitance of a FET transistor to thereby decrease the loading effect due to the parasitic capacitance. Now referring back to the Yamamoto disclosed teaching of figure 12, an inductor is in fact connected to a FET transistor, while Yamamoto explains that the object of that inductor is to improve the stability of the FET (Column 13, Lines 65-67; Column 14, Lines 1-6), Yamamoto does not go into explicit scientific detail as to why an inductor would in fact improve the stability factor of the FET. For that reason the examiner has supplied the Pugel reference to explicitly teach that by including an inductor connected to a FET the stability factor may be improved by "tuning-out" the parasitic capacitance of a circuit when that circuit approaches and achieves resonance.

Therefore the examiner has supplemented the Yamamoto reference with the Pugel teachings to better clarify that the inductor in both cases is serving the same purpose, and coincidently reads on the applicant's claim. Furthermore to address the applicant's concern that the examiner is trying to combine bodily combinations of the two piece of prior art this is not the case. The examiner is supplementing the Yamamoto reference with an additional teaching of why to use an inductor in conjunction with a FET.

Regarding claims 2-4, 6-7, 9-11 & 13-21, as the examiner maintains that the rejection of claims 1 & 8 is proper those dependent claims and independent claim 15 remain rejected for the reasons cited above.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTIAN A. HANNON whose telephone number is (571)272-7385. The examiner can normally be reached on Mon. - Fri. 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ed Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C. A. H./
Examiner, Art Unit 2618
March 21, 2008

/Edward Urban/

Supervisory Patent Examiner, Art Unit 2618